USAELRDL Technical Report 2339

TECHNOLOGY FOR PNP PLANAR SILICON TRANSISTORS: SWITCHING & AMPLIFYING

Armond P. LaRocque, Robert S. Yatsko, Alex Rogel,

Raymond Jackson, Vincent E. Rible

March 1963

UNITED STATES ARMY

ELECTRONICS RESEARCH AND DEVELOPMENT LABORATORY

FORT MONMOUTH, N.J.

U. S. ARMY ELECTRONICS RESEARCH AND DEVELOPMENT LABORATORY
FORT MONMOUTH, NEW JERSEY

March 1963

USAELRDL Technical Report 2339 has been prepared under the supervision of the Director, Electronic Components Department, and is published for the information and guidance of all concerned. Suggestions or criticisms relative to the form, contents, purpose, or use of this publication should be referred to the Commanding Officer, U. S. Army Electronics Research and Development Laboratory, Fort Monmouth, New Jersey, Attn: Chief, Semiconductor and Microelectronics Branch, Solid State and Frequency Control Division.

J. M. KIMBROUGH, JR.
Colonel, Signal Corps
Commanding

OFFICIAL:
HOWARD W. KILLAM
Major, SigC
Adjutant

DISTRIBUTION:
Special

TECHNOLOGY FOR PNP PLANAR SILICON TRANSISTORS: SWITCHING & AMPLIFYING

Armond P. LaRocque, Robert S. Yatsko, Alex Rogel,
Raymond Jackson, Vincent E. Rible

DA TASK NR. 3A99-21-003-02

ABSTRACT

Processes and techniques required for fabrication of experimental planar PNP silicon transistors have been developed and demonstrated as feasible. Processes involved include material preparation, antimony base diffusion, boron emitter diffusion, oxide masking, photoresist techniques, simultaneous gold metalizing of emitter and base regions, collector alloy contact and basing, and thermocompression bonding. Initial transistors have typical dc Beta values of 35 to 40 and F_T values as high as 350 MCS.

Processes described have also been used in preliminary fabrication of solid-state microcircuit passive components.

U. S. ARMY ELECTRONICS RESEARCH AND DEVELOPMENT LABORATORY
FORT MONMOUTH, NEW JERSEY

CONTENTS

LIST OF FIGURES

TECHNOLOGY FOR PNP PLANAR SILICON TRANSISTORS: SWITCHING & AMPLIFYING

INTRODUCTION

Despite the large number of publications and presentations concerning processes for fabricating NPN silicon transistors, relatively little information has been disseminated on techniques for preparing PNP silicon transistors, particularly double diffused planar types.

It is the purpose of this report to describe the various processes and techniques developed at USAELRDL to fabricate planar PNP silicon transistors. Included are discussions of material preparation, antimony base diffusion, boron emitter diffusion, photoresist techniques for preparing oxide masks, vacuum metalizing of contacts to the diffused regions and collector bulk material, transistor basing, and thermocompression bonding to the metalized regions.

DISCUSSION

Material Preparation

Wafers used in these experiments were prepared from 1 ohm-cm p-type single crystals grown by the Czochralski method, using needle-form seeds to minimize dislocations. Crystals were grown in a USAELRDL-designed and fabricated furnace which uses resistance heating.[1] The temperature monitored one-half inch below the quartz crucible was lowered from 1408° to 1382°C during crystal pulling. The needle-form seed was rotated at 14 rpm. with a drawing rate of 4 inches per hour. Dried argon gas was passed through the chamber at the rate of 20 cfh. The resulting crystals were approximately 3/4 inch in diameter with a dislocation density of 100-1000/ sq cm.

The wafers were sliced in the [111] plane to a thickness of .020 inches and lapped with 1000 grit Al_2O_3 to a thickness of .012 inches to remove saw damage. One face of each wafer was then mechanically polished to an optical finish using either one-quarter micron diamond paste or one-tenth micron synthetic sapphire.[2] When the diamond paste was used, extremely fine scratches were discernible under high-powered magnification with dark-field illumination. Similar examination disclosed an extremely fine "orange-peel" effect upon use of the latter polishing compound. Neither surface condition had a deleterious effect on the planarity of the diffused junctions.

Following surface polishing, the wafers were thoroughly cleaned in organic solvents according to the schedule in Table I.

TABLE I

SOLVENT	TIME	REMARKS
Toluene	5 min.	Heat to boiling and ultra-sonorate
Amyl acetate	5 min.	Rinse, heat to boiling and ultra-sonorate
Acetone	5 min.	" "
Ethyl alcohol	5 min.	" "
High resistivity water	5 min.	Rinse, heat to boiling and ultra-sonorate
Hydrofluoric acid	5 min.	Soak at room temperature
High resistivity water	5 min.	Boil, then blot on lint-free paper

Following the above cleaning, the wafers were ready for oxidation. This was accomplished by heating the wafers in a steam atmosphere at 1100°C for 25 minutes, resulting in a second-order purple oxide approximately 2800 Å thick. Upon formation of this oxide, wafers were ready for the initial mask which defined the area into which antimony was diffused to form the base-collector junction. This was accomplished by using photoresist films as discussed in the following section.

Photoresist Process

In the photoresist process Kodak Photoresist (KPR), diluted 10 parts to 1 part KPR thinner, was applied with an eyedropper to the clean, freshly oxidized wafers which had been placed on a slinger. To prevent dust particles from settling on the drying film of KPR, the slinger is kept within a plexiglas box in which dry argon constantly flows. The photoresist process was conducted as described in Table II.

TABLE II

STEP NO.	REMARKS
1.	Coat wafer and spin for 5 seconds at 320 rpm at a radius of 2 1/2 inches.
2.	Dry at room temperature inside plexiglas box for 1 minute.
3.	Bake in oven at 120°C for 10 minutes.

TABLE II
(Cont)

STEP NO.	REMARKS
4.	Expose to ultraviolet light for 3 minutes. Light source is a Hanovia Compact Arc XeHg 1000 watt lamp.
5.	Develop in Kodak KPR developer for 3 minutes, rinse in 50-50 ethyl alcohol-water solution until clean. Dry under infrared for 1 minute.
6.	Bake in oven at 220°C for 10 minutes.
7.	Dissolve oxide in a solution of 30 gms ammonium fluoride, 60 cc water and 9 cc hydrofluoric acid.
8.	Remove KPR by soaking in hot sulfuric acid, rinse in high resistivity water and dry under infrared for 10 minutes.

The wafers were now ready for the antimony base diffusion.

Antimony Base Diffusion

The preliminary work done on the diffusion of antimony into silicon disclosed that surface damage could be eliminated by the use of an oxide source, an oxidized silicon surface and an oxidizing atmosphere.[3] It was also determined that masking of antimony during a conventional one-step process was well-nigh impossible.

The base-collector junction was formed by a two-step process using antimony as the diffusant. Two steps were necessary since a continuous diffusion resulted in a carrier concentration (2×10^{19} donor atoms/cc) which was too high for the base region and caused breakdown of the oxide mask. The diffusion schedule is given in Table III.

TABLE III

STEP NO.	REMARKS
1.	Pre-deposition: Sb_2O_3 at 790°C in a stream of argon passed through high resistivity water at 25°C, argon flow rate being 1 liter/min. Silicon heated at 1100°C for 20 min without pre-heating, cooled at 3°C per minute to 1050°C, the temperature at which the emitter diffusion takes place, and then air-quenched to room temperature.

TABLE III
(Cont)

STEP NO.	REMARKS
1.	Oxide formed within the base region is the first-order blue of 950 Å.
2.	Oxide removed in ammonium fluoride solution listed above for approximately 4 minutes. The antimony-silicon oxide within the base region was completely removed while the thicker oxide mask was reduced to an antimony-free oxide of the first-order blue.
3.	Redistribution: Silicon heated at 1225°C for 2 hours, in air, without preheating. Cooled at 3°C per minute to 1050°C and air-quenched to room temperature.

Following the pre-deposition step, the antimony junction occurred at a depth of 0.3 microns while the carrier concentration was approximately 10^{19} donor atoms/cc. No evidence of antimony diffusion through the oxide mask has been detected.

Following the redistribution step, the oxide within the base region was the second-order red of 2550Å and served as the mask for the boron emitter diffusion. This red oxide contrasted with the blue oxide over the remainder of the wafer and facilitated subsequent registration.

The base region had a typical junction depth of 2.3 microns. The surface sheet resistance was approximately 175 ohms per square with a surface concentration of 2×10^{18} donor atoms per cc and a typical BV_{CBO} of 45 volts at 10-8 amperes.

After the antimony base diffusion was completed, the oxide mask, to permit localized boron diffusion for the emitter, was formed by the photoresist process described above.

Boron Emitter Diffusion

The choice of the impurity for use as a p-type emitter in a PNP planar silicon transistor was limited to boron in order to achieve the high surface concentration needed for high injection efficiency, namely, greater than 10^{20} acceptor atoms/cc. Other acceptor atoms, such as indium, gallium, and aluminum do not generally yield such high surface concentrations. A high surface concentration was not the only criterion of a good emitter dopant, however. Junction planarity, control of surface perfection, diffusion control, and reproducibility and ability to be masked by an oxide

film were all factors which had to be considered. It was determined that boron met all the above requirements, but boron diffusion techniques previously employed were either inadequate or too cumbersome.

A modification of a technique first proposed by D'Asaro[4] was adopted. This method appeared to be most suitable due to its relative simplicity and its efficiency in meeting the requirements of the p-type emitter. A detailed description of this modified closed-box system and the experimental results obtained using this technique for boron diffusion has been reported from these aboratories.[5] A description of the apparatus need not be given, therefore, but the procedures involved and the experimental results, as applied specifically to the formation of the emitter of the PNP transistor, are given below.

Following preparation of the oxide mask, the wafers were cleaned using the method given in Table I. The wafers were then thoroughly dried at 120°C for 15 minutes, and boron was then diffused following the procedure set forth in Table IV.

TABLE IV

STEP NO.	REMARKS
1.	Furnace temperature set at 1025°C and flushed with dry argon at 1 liter/min for 30 min.
2.	Insert diffusion apparatus, containing B_2O_3 source and wafers, into cool end of furnace and flush with dry argon for 20 minutes.
3.	Diffusion apparatus moved into hot zone of furnace. Wafers and source are now at 1025°C.
4.	Diffuse for 50 minutes. Argon flow continues.
5.	Cool at rate of 2°C/min until 700°C is reached.
6.	Remove from furnace and cool to room temperature. Open box and remove wafers.

The diffusion process described above resulted in an oxide which was the second-order clear blue of 1100Å within the emitter regions. This was adequate to serve as a mask against metalizing a contact to the emitter. The oxide over the remainder of the wafer was not visibly altered.

The emitter region had a typical junction depth of 1.3 microns. The

surface sheet resistance was approximately 9.5 ohms per square with a surface concentration of approximately 2×10^{20} acceptor atoms per cc and a typical BV_{EBO} of 6 volts at 10^{-8} amperes.

Following the formation of the two diffused junctions, the oxidized wafers were treated with the photoresist process to provide a mask for contact metalizing.

Vacuum Metalizing

Contacts to the emitter and base regions were formed by the simultaneous evaporation and alloying of 1% Sb-Au to the silicon diffused regions where the oxide had been removed during the photoresist process. The remaining oxide served to prevent the doped gold from wetting the surface junction regions and thus prevented emitter-base shorts.

The process used for metalizing is given in Table V.

TABLE V

STEP	Tsi	TIME	REMARKS
1.	Normal Room Ambient	1 min.	Outgas and premelt Sb-Au wire loops which are draped on tungsten coil. Shield silicon wafer.
2.	700°C	15 min.	Outgas molybdenum heater platform and silicon wafer. Sb-Au allowed to cool.
3.	700°C	2 min.	Reheat Sb-Au and remove shield from silicon wafer.
4.	700°C	3 min.	Evaporate Sb-Au onto heated silicon.
5.	600°C	2 min.	Continue evaporation.
6.	500°C	4 min.	Continue evaporation.
7.	400°C	2 min.	Complete evaporation.
8.	200°C	10 min.	Silicon allowed to cool to room temperature after this annealing period.

A typical metalizing process used 22 cm of .030-in.-diameter 1% Sb-Au wire heated on a .020-in. tungsten filament which was 5 in. from the silicon. This resulted in a deposit which was calculated to be 4600Å. It should be noted that the 5-in. distance was necessary in order to insure the easy removal of the gold film from the oxide by swabbing with acetone. When the gold source was placed within 4 in., the gold appeared to wet the oxide and complete removal was impossible without disturbing the gold film on the alloyed contact regions.

Determination of the exact amount of antimony remaining in the gold, after initial outgassing and pre-melting, and hence available for the contact, was not practical. It was determined experimentally, however, that the residual antimony was sufficient to result in a lower resistance contact than that achieved through the use of pure gold. The amount of antimony was small enough to yield a very low resistance ohmic contact to both the heavily doped p-type emitter and the lower doped n-type base. The top of the gold contacts provided an excellent surface for lead wire application by thermocompression bonding.

Contact to the collector was made by evaporating 2.5% Ga-Au to the freshly lapped silicon surface on the under (collector) side of the wafer.

The process used for metalizing is given in Table VI.

TABLE VI

STEP	Tsi	TIME	REMARKS
1.	Normal Room Ambient	2 min.	Outgas and premelt Ga-Au wire loops. Shield silicon.
2.	100°C	2 min.	Remove shield and start evaporation of Ga-Au.
3.	150°C	5 min.	Complete evaporation.
4.	200°C incl. to 350°C	3 min.	Continue tungsten filament voltage to provide radiant heating of Ga-Au surface.
5.	- - -	10 min.	Allow silicon to cool to room temperature.

A typical metalizing process used 22 cm of .020-in.-diameter 2.5% Ga-Au wire heated on a .020" tungsten filament which was 2 in. from the silicon. The heat radiated from the filament was enough to heat the silicon and its support platform to the thermocouple-indicated temperatures given above. This temperature range was high enough to effect a tenacious bond of the gold to the silicon. Actual alloying was brought about during the basing operation.

The transistor dice were affixed to TO-5 headers by heating the headers in a stream of forming gas at 380° long enough to melt a thin wafer of cadmium metal. At this point, the cadmium alloyed with the gold plated header and the silicon-gallium-gold alloyed collector surface, providing an excellent physical and electrical bond between die and header. The transistor and header were then cooled to 310°C, at which point .001-in. wires were bonded to the emitter and base contacts by the standard thermocompression technique.

Design and Evaluation Data

The first of two designs used in fabricating a planar PNP silicon transistor is shown in Fig. 1. The collector junction was a 24-mil square with a rectangular emitter of 6 x 18 mils having a contact stripe of 2 x 12 mils. There were base contact stripes of 4 x 18 mils on either side of the emitter.

These transistors, with a nominal base width of 1 micron, had typical Betas of 35 to 40, as shown in Fig. 2. The reverse characteristics of the two diodes are shown in Fig. 3a and 3b. It can be seen that BV_{CBO} = 40 volts and BV_{EBO} = 5 volts. Transistors of this first design yielded F_T values of approximately 190 Mcs with a collector dissipation of 1/2 watt. The output capacitance at 1 Mc was approximately 60 μμf with 0.5 volt bias.

The second design is shown in Fig. 4. The collector junction was teardrop shaped with an 8-mil diameter, in the center of which was a 4-mil-diameter circular emitter. Contact was made to a 2-mil dot within the emitter and to a 1.5-mil ring within the base region outside the emitter periphery. These transistors, with a nominal base width of 1 micron, had typical Betas of 35 to 40, as shown in Fig. 5. The diode reverse characteristics are shown in Fig. 6a and 6b. It can be seen that BV_{CBO} = 47 volts and BV_{EBO} = 6 volts. Transistors of this second design yielded F_T values of approximately 250 Mcs with a collector dissipation of 1/4 watt. The output capacitance at 1 Mc was approximately 9 μμf with a 0.5 volt bias. These transistors had power gain of 25 db at 30 Mcs.

The same technology using commercially obtained epitaxial material and the geometry of Fig. 4 produced good switching transistors. Betas dropped to around 15 due to poor lifetime, but a base width narrowed to one half micron yielded correspondingly higher F_T values (350 mc) and good switching times. With no capacitors in the circuit, a base current of 2.5 ma and a collector current of 10 ma (overdrive factor of 3.75) produced a delay time of 20 nsec, a rise time of 23 nsec, a storage time of 100 nsec, and a fall time of 60 nsec for a total of 203 nsec switching time. The addition of an attenuating capacitor virtually eliminated storage time and reduced delay time to 4 nsec, rise time to 9 nsec, fall time to 10 nsec, for a total of 23 nsec.

Passive Circuit Components

The present trend in microelectronics is the use of solid-state integrated circuits incorporating both active and passive components fabricated as integral parts of the semiconductor substrate. Several manufacturers have demonstrated the feasibility of fabricating passive components using processes and techniques simultaneously with the fabrication of the active devices. These integrated circuits, using NPN silicon planar transistors, have been shown to be reliable and of high quality.

Following fabrication of the described transistors, some preliminary experiments were conducted to adapt transistor fabrication processes to the fabrication of resistors and capacitors for use in PNP integrated circuits. The initial experiments were confined to fabricating capacitors by the deposition of aluminum onto typical oxides grown during transistor fabrication. Typically, 4 cm of .030-in.-diameter aluminum were evaporated from a distance of 2 in. to give a film approximately 5000Å thick. The process used is given in Table VII.

TABLE VII

STEP	Tsi	TIME	REMARKS
1.	Normal Room Ambient	2 min.	Outgas and premelt Al wire with silicon wafer shielded.
2.	350°C	20 min.	Outgas oxidized wafer.
3.	100°C	4 min.	Evaporate aluminum.
4.	----	10 min.	Cool to room temperature.
5.	----	----	Coat with KPR and expose for desired pattern.
6.	----	----	Remove aluminum where so desired with 10% NaOH for 3 minutes.
7.	----	----	Remove KPR with H_2SO_4 and clean.
8.	----	----	Back of wafer is lapped and pure gold contact is made as per process in Table VI.

The resulting aluminum films had a mirror-like appearance and a tenacious bond to the oxide. The optimum aluminum film thickness and vacuum processing have yet to be determined in order to minimize variations in capacitance and resistance for predetermined oxide films. Variations in permittivity, as related to manner of oxide growth, doping level, and type of silicon, have yet to be determined.

Preliminary experiments have yielded capacitors having a capacitance range of 30-40,000 $\mu\mu f/cm^2$ and a shunt resistance of 10-100 kilohms with thermally grown oxides of 800Å thickness. Capacitors with thermally grown oxides of 2900Å thickness have had a capacitance range of 8-12,000 $\mu\mu f/cm^2$. These values are for capacitors which were .058 in. square and were measured at 100 KC using a Model 74C-S8 Boonton Capacitance Bridge. A typical capacitor is shown in Fig. 7.

In addition to the preliminary work on capacitors, some initial

experiments have been conducted on the preparation of diffused resistors. Fig. 8 is a photograph of a resistor formed during a typical antimony base diffusion. Each leg is .0015 in. wide and .050 in. long with a resistance of approximately 5 kilohm. The sheet resistance of these resistors is 175 ohms per square with a resistivity of approximately .04 ohm-cm. Reducing the surface concentration by an order of magnitude to 10^{17} atoms/cc increases the resistance by a factor of 4. The preliminary data obtained indicates that with the use of proper photoresist transparencies it should be possible to form fine-line diffused resistors of 10 megohms in 1 cm^2 of surface area. Contact to the resistors can be made by the use of photo-resist to remove the oxide wherever desired and metalizing by the method described in Table V. The value of the oxidized resistor is unaffected by subsequent exposure to the emitter diffusion process.

CONCLUSIONS

It can be concluded from a study of devices which were successfully fabricated that the aforementioned processes are appropriate for the production of high-frequency planar PNP silicon transistors. It is believed that further improvement in frequency response can be achieved by a reduction in junction areas and improvement in the grounded emitter current gain achieved by a reduction in base width.

The effort in passive component fabrication is admittedly preliminary, but initial experiments indicate the compatibility of planar PNP transistor fabrication with that of associated passive components for the preparation of semiconductor integrated circuits. It is felt that integrated circuits containing high frequency double diffused silicon planar transistors will have applicability in military electronics as replacements for existing circuits using germanium PNP transistors. Such circuits will also be useful wherever PNP - NPN complementary circuits are desired.

ACKNOWLEDGMENTS

Grateful acknowledgment is made to W. R. Cherry for his encouragement; to W. Pharo and M. Palmateer for silicon preparation; to N. Korolkoff for the photographic presentations; and to K. Fischer and W. Spry for the device evaluation data.

REFERENCES

1. "Silicon Pulling Furnace," by W. B. Pharo and W. R. Cherry, presented at Electrochemical Society meeting in Cincinnati, Spring 1955.

2. "Lapping and Polishing of Silicon Monocrystals," W. B. Pharo, USASRDL Technical Report 2188, April 1961.

3. "Diffusion of Antimony Into Silicon through an Oxide Layer," by A. P. LaRocque, R. S. Yatsko and A. Quade. Presented at Electronics Division Semiconductor Symposia of the Electrochemical Society in Ottawa, Canada, Autumn 1958.

4. "Diffusion and Oxide Masking in Silicon by the Box Method," by L. A. D'Asaro. Solid-State Electronics, Vol. 1 pp. 3-12, March 1960.

5. "A Modified Closed Box System for the Diffusion of Boron in Silicon," by R. S. Yatsko and J. S. Kesperis, Journal Electrochemical Society, Vol. 107, No. 11, November 1960.

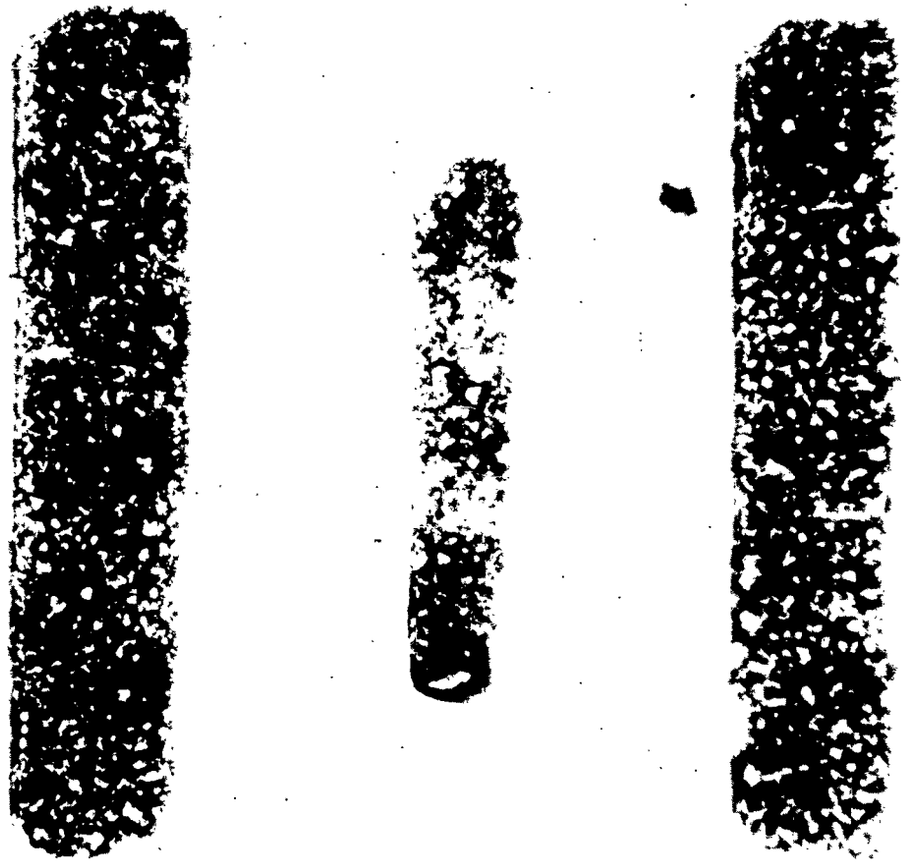
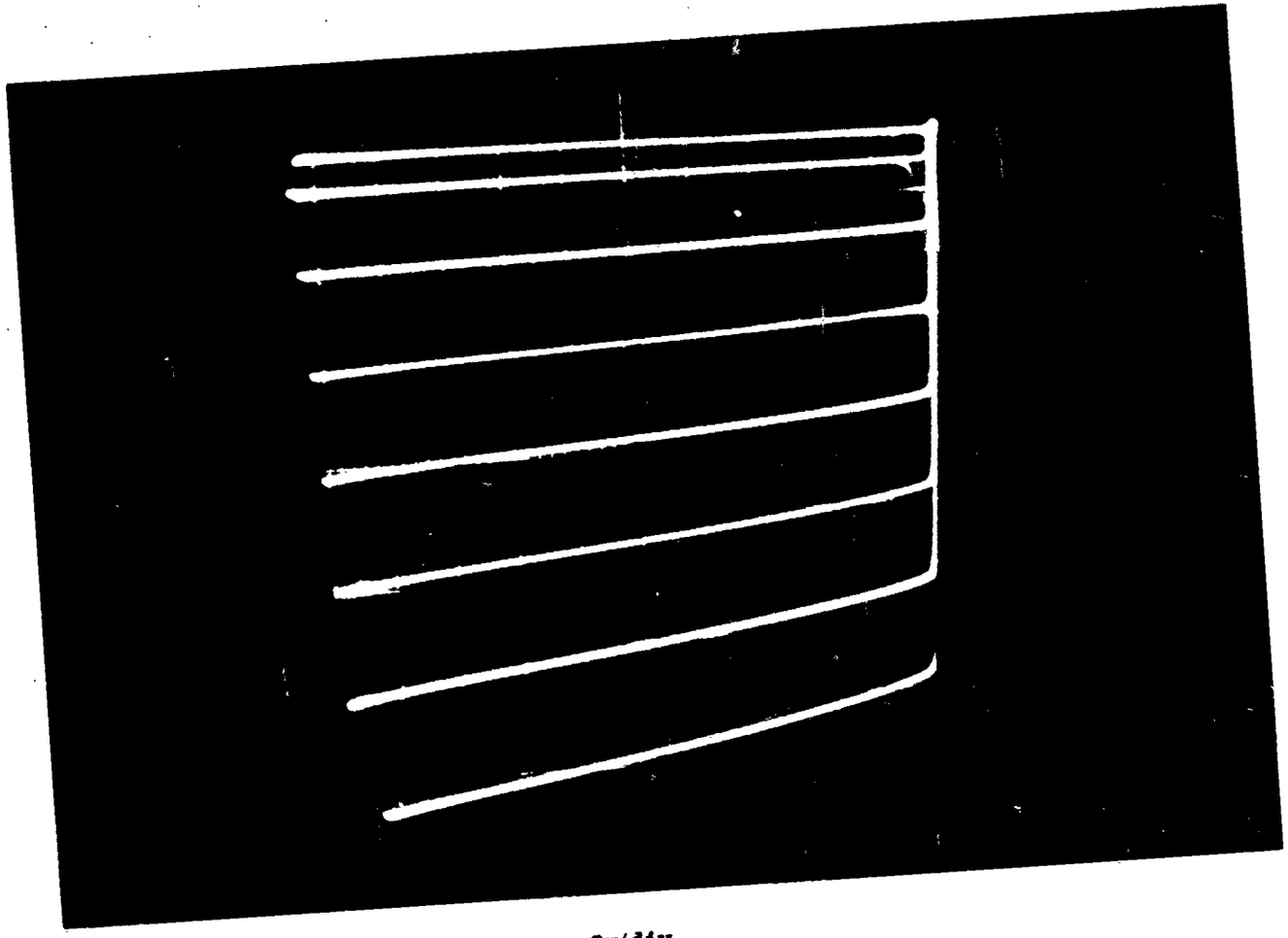
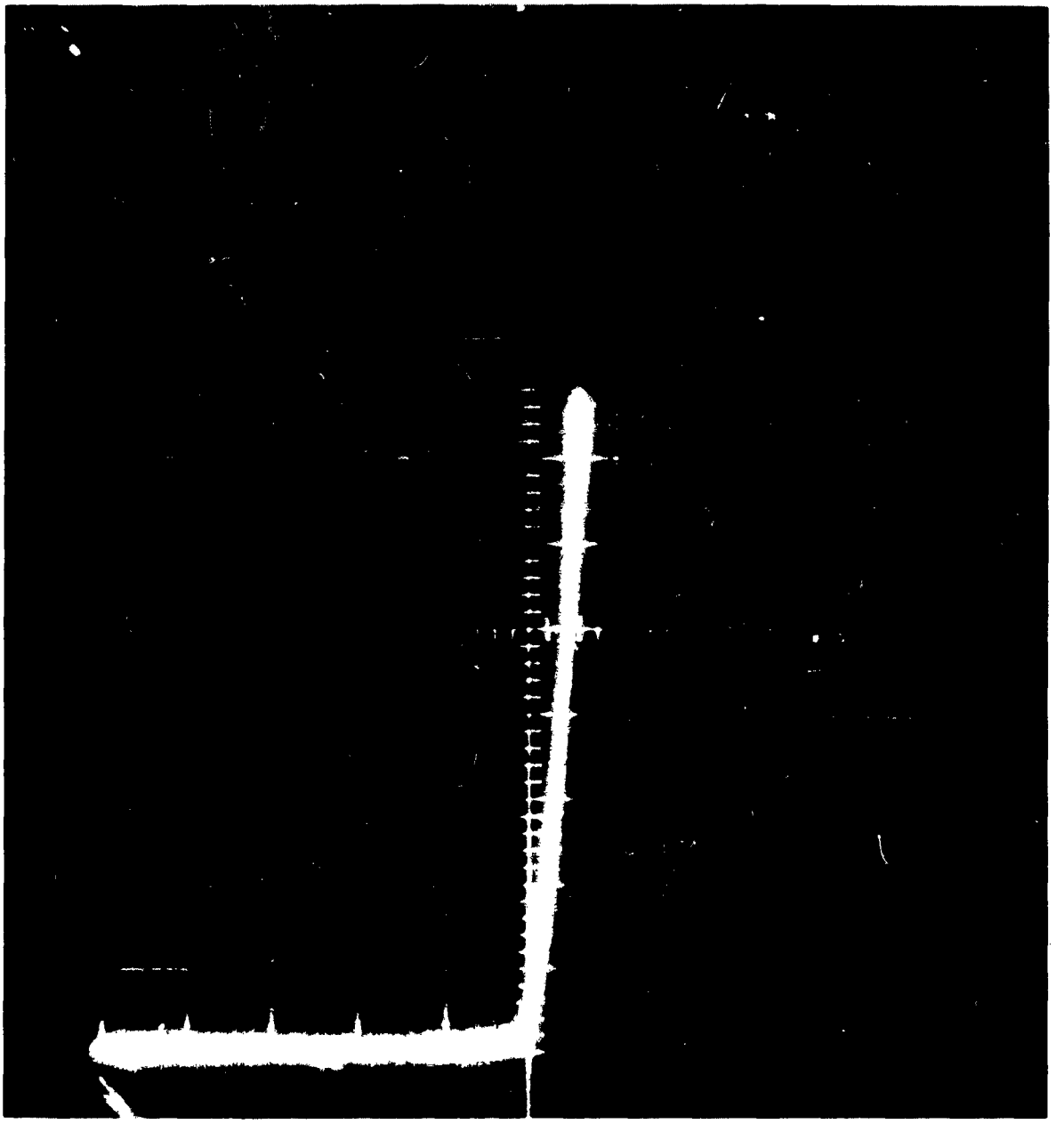


FIGURE 1 TRANSISTOR DESIGN NO. 1



Abscissa: 2v/div.
Ordinate: .2ma/div.
Selector: .01ma/step

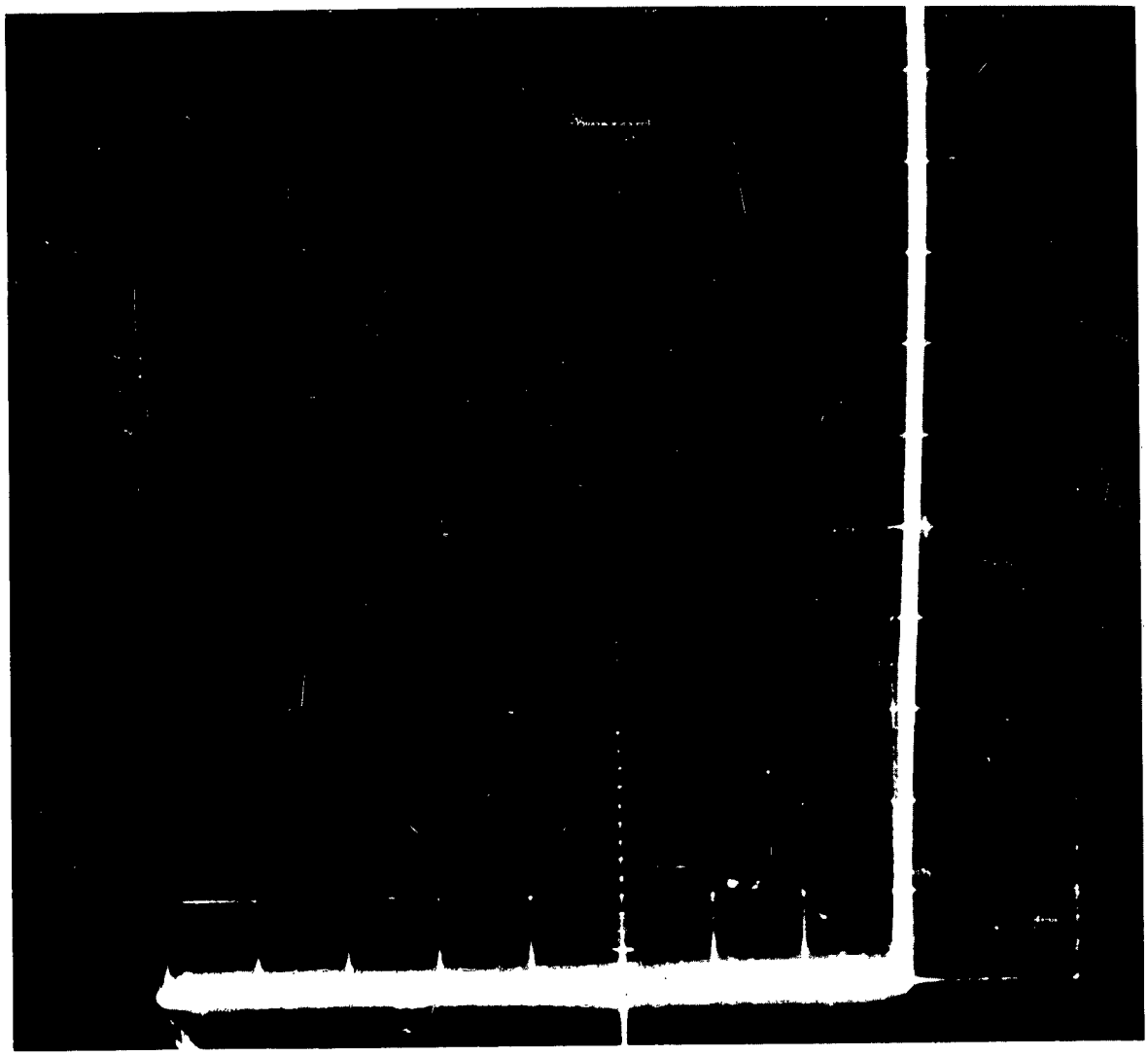
FIGURE 2 BETA FOR TRANSISTOR NO.1



BV_{EBO}

Abscissa: 1v/div.
Ordinate: .01ma/div.

FIGURE 3a. EMITTER-BASE DIODE, TRANSISTOR NO.1



BV_{CBO}

Abscissa: 5v/div.
Ordinate: .01ma/div

FIGURE 3b. COLLECTOR-BASE DIODE, TRANSISTOR NO. 1

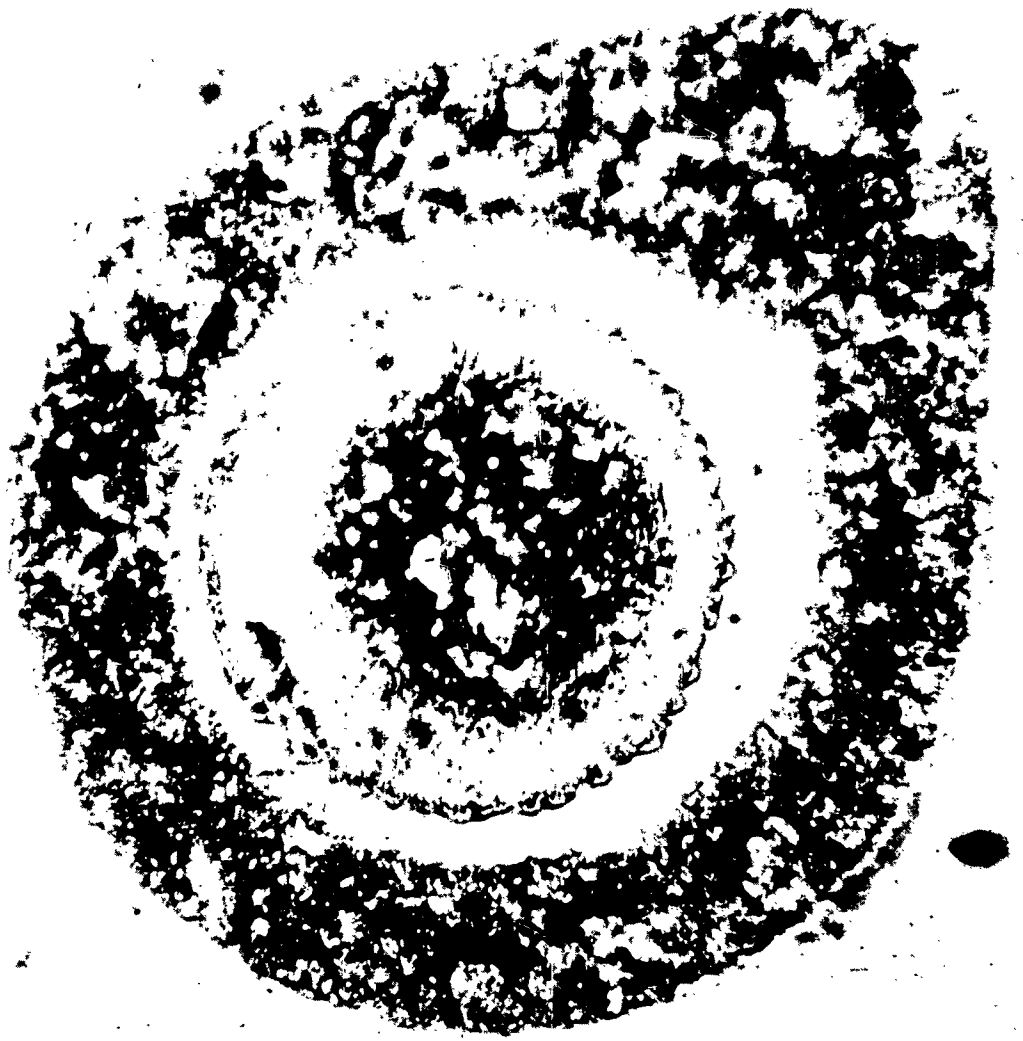
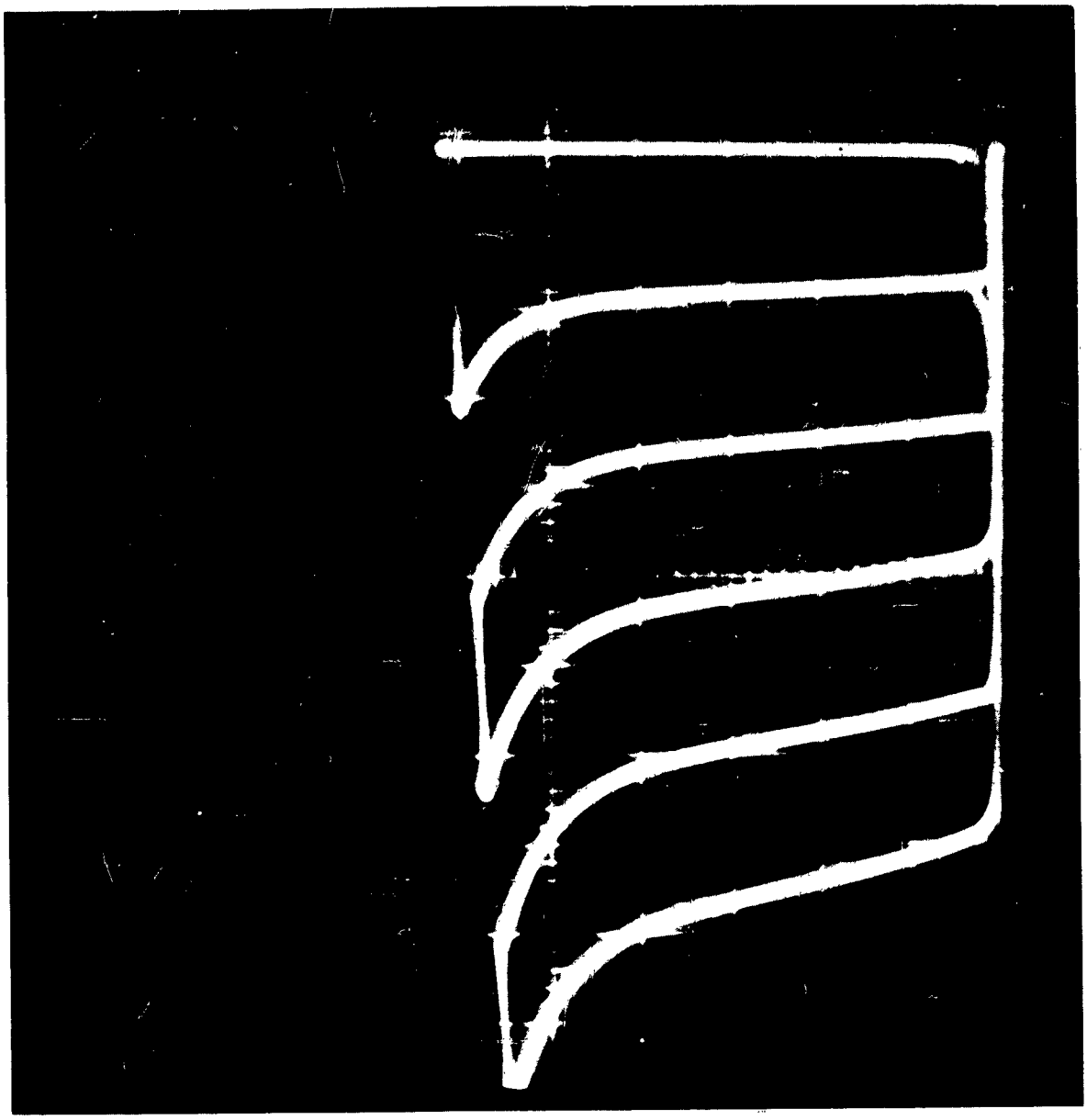
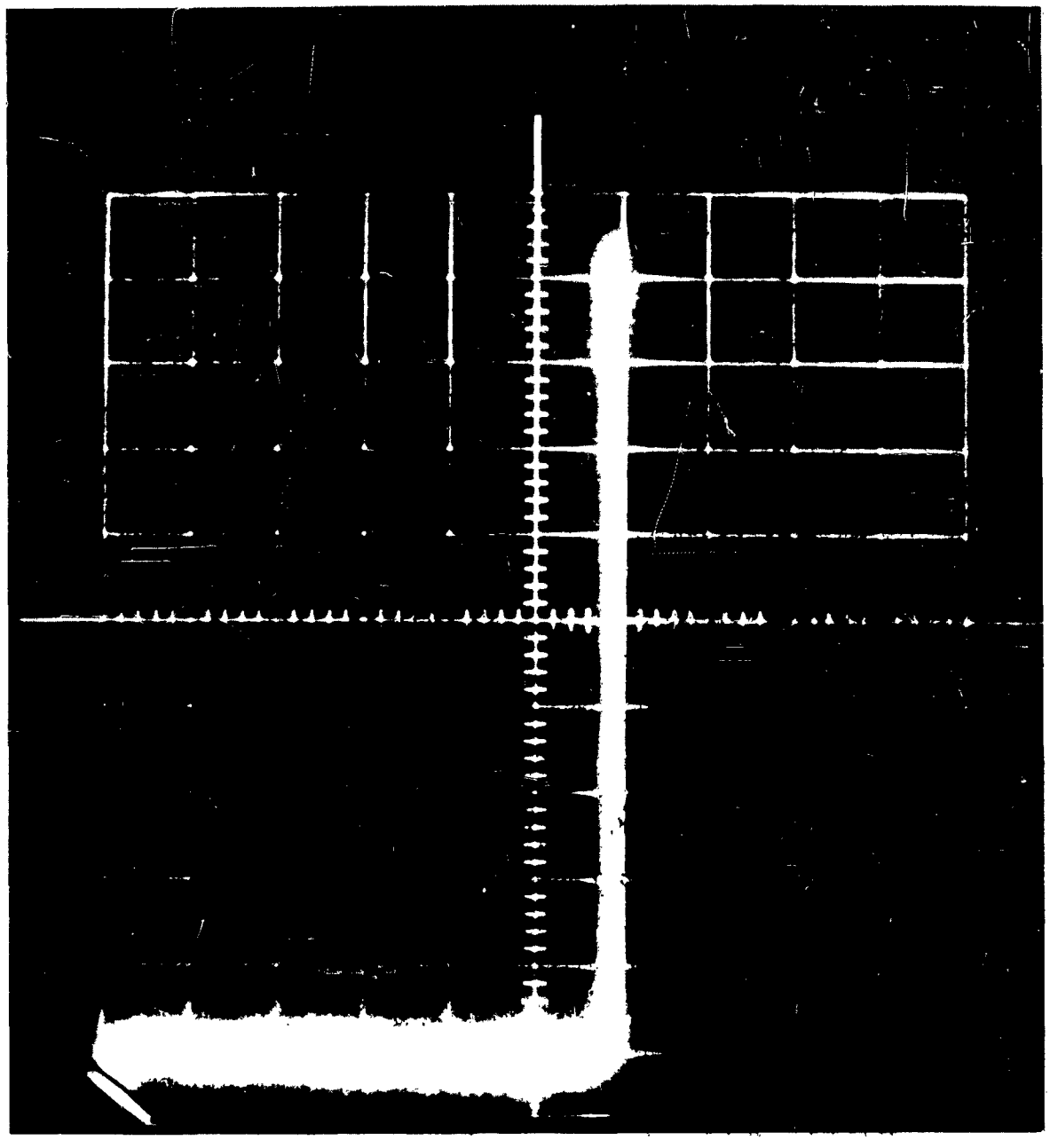


FIGURE 4 TRANSISTOR DESIGN NO. 2



Abscissa: 5v/div.
Ordinate: .2ma/div.
Selector: .01ma/div.

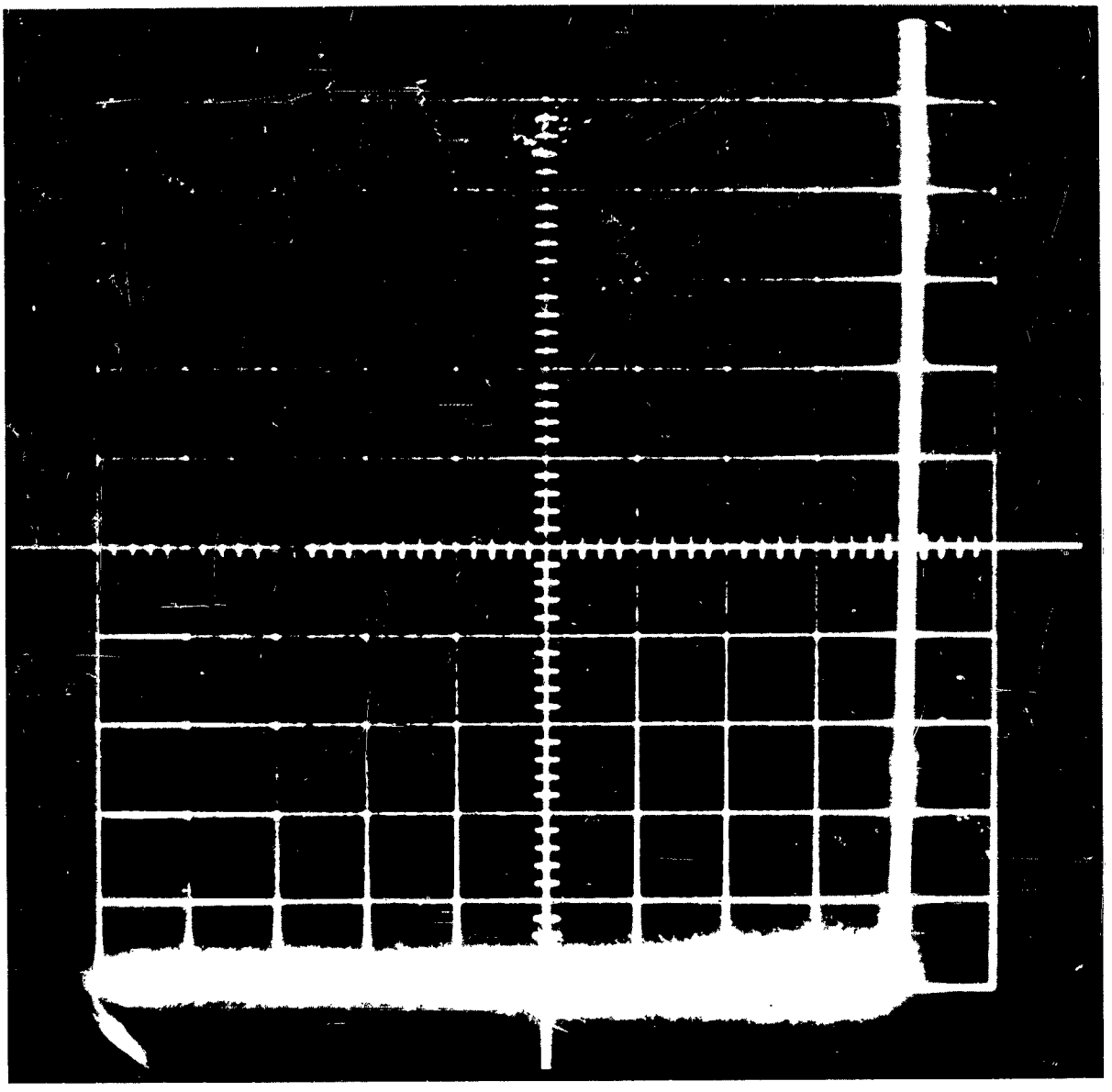
FIGURE 5 BETA FOR TRANSISTOR NO.2



BV_{EBO}

Abscissa: 1v/div.
Ordinate: .01ma/div.

FIGURE 6a. EMITTER-BASE DIODE, TRANSISTOR NO.2



BV_{CBO}

Abscissa: 5v/div.
Ordinate: .01ma/div.

FIGURE 6b. COLLECTOR-BASE DIODE, TRANSISTOR NO.2

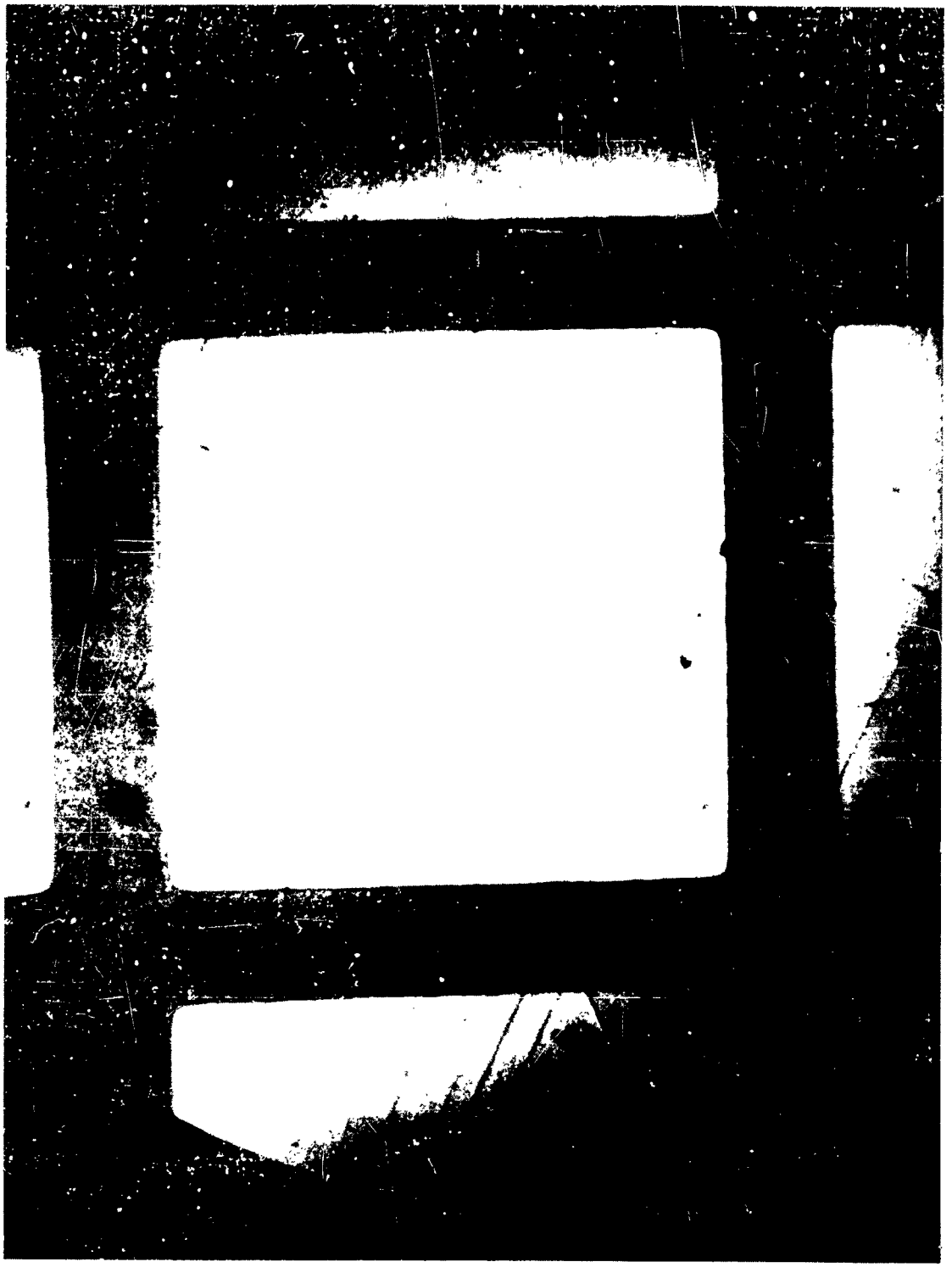


FIGURE 7. ALUMINUM-SILICON DIOXIDE-SILICON CAPACITOR

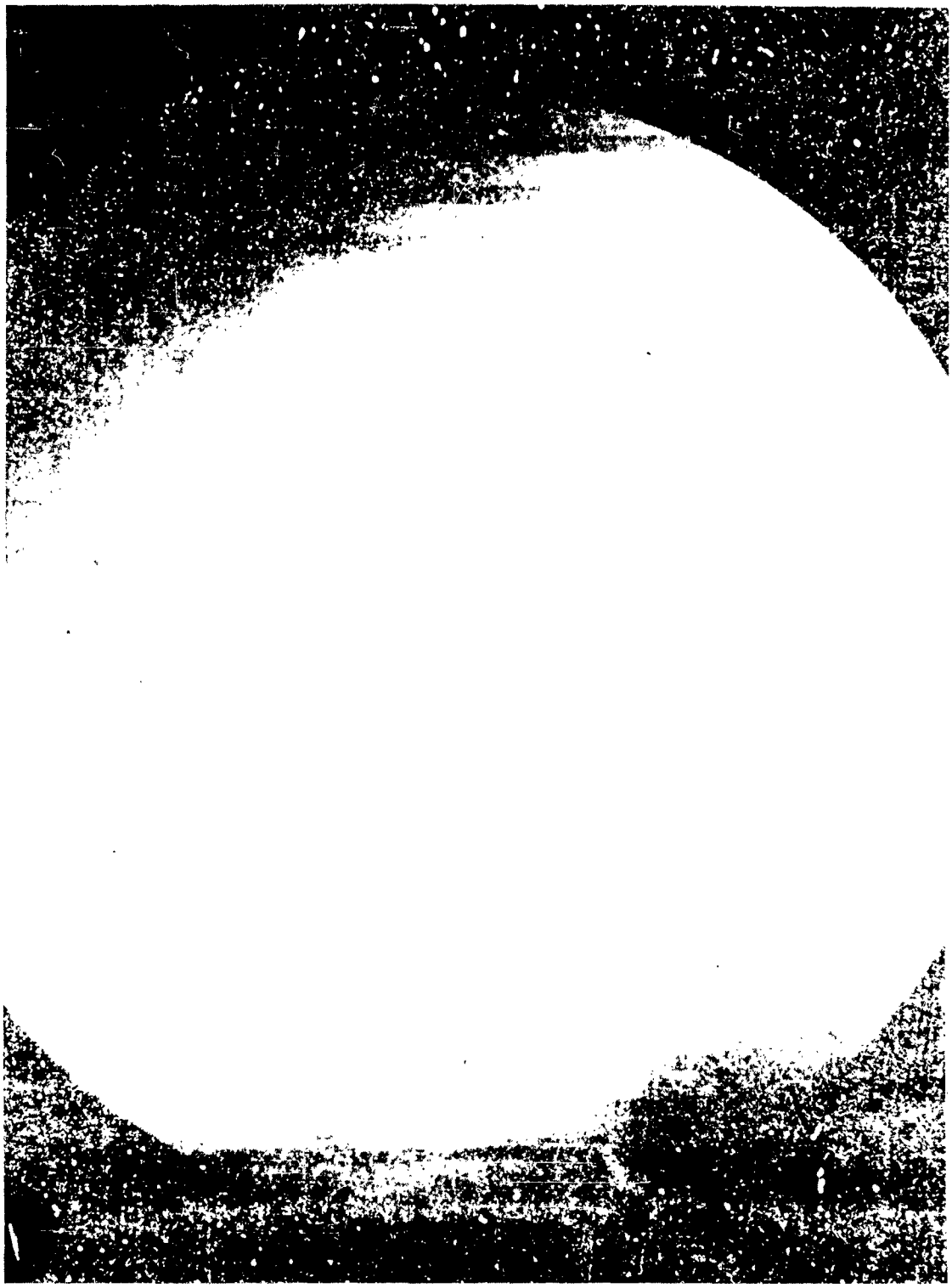


FIGURE 8. DIFFUSED SILICON RESISTOR

DISTRIBUTION

	COPIES
Commanding General U. S. Army Electronics Command ATTN: AMSEL-AD Fort Monmouth, New Jersey	3
Office of the Assistant Secretary of Defense (Research and Engineering) ATTN: Technical Library Room 3E1065, The Pentagon Washington 25, D.C.	1
Chief of Research and Development Department of the Army Washington 25, D. C.	2
Chief, United States Army Security Agency ATTN: ACofS, G4 (Technical Library) Arlington Hall Station Arlington 12, Virginia	1
Commanding Officer U. S. Army Electronics Research & Development Activity ATTN: Technical Library Fort Huachuca, Arizona	1
Commanding Officer U. S. Army Electronics Research & Development Activity ATTN: SELWS-AJ White Sands, New Mexico	1
Commanding Officer U. S. Army Electronics Research Unit P. O. Box 205 Mountain View, California	1
Commanding Officer U. S. Army Electronics Materiel Support Agency ATTN: SELMS-ADJ Fort Monmouth, New Jersey	1
Commanding General U. S. Army Satellite Communications Agency ATTN: Technical Documents Center Fort Monmouth, New Jersey	1

DISTRIBUTION (Cont)

	COPIES
Commanding Officer U. S. Army Engineer Research & Development Laboratories ATTN: Technical Documents Center Fort Belvoir, Virginia	1
Commanding Officer U. S. Army Chemical Warfare Laboratories ATTN: Technical Library, Building 330 Army Chemical Center, Maryland	1
Commanding Officer Harry Diamond Laboratories ATTN: Library, Building 92, Room 211 Washington 25, D.C.	1
Headquarters, United States Air Force ATTN: AFCIN Washington 25, D.C.	2
Rome Air Development Center ATTN: RAALD Griffiss Air Force Base New York	1
Headquarters Ground Electronics Engineering Installation Agency ATTN: ROZMEL Griffiss Air Force Base, New York	1
Commanding General U. S. Army Materiel Command ATTN: R&D Directorate Washington 25, D.C.	2
Aeronautical Systems Division ATTN: ASAPRL Wright-Patterson Air Force Base, Ohio	1
U. S. Air Force Security Service ATTN: ESD San Antonio, Texas	1
Headquarters Strategic Air Command ATTN: DOCE Offutt Air Force Base, Nebraska	1

DISTRIBUTION (Cont)

	COPIES
Headquarters Research & Technology Division ATTN: RTH Bolling Air Force Base Washington 25, D.C.	1
Air Proving Ground Center ATTN: PGAPI Eglin Air Force Base, Florida	1
Air Force Cambridge Research Laboratories ATTN: CRXL-R L. G. Hanscom Field Bedford, Massachusetts	2
Headquarters Electronic Systems Division ATTN: ESAT L. G. Hanscom Field Bedford, Massachusetts	2
AFSC Scientific/Technical Liaison Office U. S. Naval Air Development Center Johnsville, Pa.	1
Chief of Naval Research ATTN: Code 427 Department of the Navy Washington 25, D.C.	1
Bureau of Ships Technical Library ATTN: Code 312 Main Navy Building, Room 1528 Washington 25, D.C.	1
Chief, Bureau of Ships ATTN: Code 454 Department of the Navy Washington 25, D.C.	1
Chief, Bureau of Ships ATTN: Code 686B Department of the Navy Washington 25, D.C.	1
Director U. S. Naval Research Laboratory ATTN: Code 2027 Washington, 25, D.C.	1

DISTRIBUTION (Cont)

	COPIES
Commanding Officer & Director U. S. Navy Electronics Laboratory ATTN: Library San Diego 52, California	1
Commander U. S. Naval Ordnance Laboratory White Oak Silver Spring 19, Maryland	1
Commander Armed Services Technical Information Agency ATTN: TISIA Arlington Hall Station Arlington 12, Virginia	20
USAELRDL Liaison Officer U. S. Army Tank Automotive Center Detroit Arsenal Center Line, Michigan	1
USAELRDL Liaison Officer Naval Research Laboratory ATTN; Code 1071 Washington 25, D.C.	1
USAELRDL Liaison Officer Massachusetts Institute of Technology Building 26, Room 131 77 Massachusetts Avenue Cambridge 39, Massachusetts	1
USAELRDL Liaison Office Aeronautical Systems Division ATTN: ASDL-9 Wright-Patterson Air Force Base Ohio	1
U. S. Army Research Liaison Office Lincoln Laboratory P. O. Box 73 Lexington, Massachusetts	1
USAELRDL Liaison Officer Rome Air Development Center ATTN: RAOL Griffiss Air Force Base, New York	1

DISTRIBUTION (Cont)	Copies
USAEIRDL Liaison Officer U. S. Army Combat Development Command, CDCLN-EL Fort Belvoir, Virginia	1
USAEMSA Liaison Engineer USASCAJ APO 343 San Francisco, California	1
Technical Director, SELRA/CS Headquarters, USAELRDL	1
USAELRDA-White Sands Liaison Office SELRA/LNW, USAELRDL	1
AFSC Scientific/Technical Liaison Office SELRA/LNA, USAELRDL	1
Corps of Engineers Liaison Office SELRA/LNE, USAELRDL	1
Marine Corps Liaison Office SELRA/LNR, USAELRDL	1
USACDC Liaison Office SELRA/LNF, USAELRDL	2
Commanding Officer U.S. Army Security Agency Processing Center Deal Area - Bldg. 5001	1
Mr. A. H. Young Semiconductor Group Code 681A1A Bureau of Ships Department of the Navy Washington 25, D.C.	1
Chief, Technical Information Division, Hq, USAELRDL	6
USAELRDL Technical Documents Center, SELRA/ADT, Hexagon	1
Director, Electronic Components Dept., USAELRDL	1
Director, Solid State & Frequency Control Div.,EC Dept.	1
Deputy Director, SS&FC Div, EC Dept.	1
Chief,Technical Staff, SS&FC Div	5
Chief,Piezoelectric Crystal & Circuitry Br, SS&FC Div	5
Chief,Semiconductor & Microelectronics Br,SS&FC Div	25
Chief,Microwave & Quantum Electronics Br,SS&FC Div	5
File Unit Nr . 1, Rm 3D-116, Hexagon	1
Chief Scientist, U. S. Army Electronics Command Attn: AMSEL-SC, Fort Monmouth, N. J.	1

AD ______________ Div. ______________

UNCLASSIFIED

Army Electronics Research and Development Laboratory, Fort Monmouth, N. J.
TECHNOLOGY FOR PNP PLANAR SILICON TRANSISTORS: SWITCHING & AMPLIFYING by Armond P. LaRocque, Robert S. Yatsko, Alex Rogel, Raymond Jackson, Vincent E. Rible, March 1963, 21 p. incl. illus. 5 refs. (USAELRDL Technical Report 2339) (DA Task 3A99-21-003-02)
Unclassified Report

Processes and techniques required for fabrication of experimental planar PNP silicon transistors have been developed and demonstrated as feasible. Processes involved include material preparation, antimony base diffusion, boron emitter diffusion, oxide masking, photoresist techniques, simultaneous gold metalizing of emitter and base regions, collector alloy contact and basing, and thermocompression bonding. Initial transistors have typical dc Beta values of 35 to 40 and F_T values as high as 350 MCS. Processes described have also been used in preliminary fabrication of solid-state micro-circuit passive components.

1. Transistors, PNP Silicon, Technology for
2. Technology, PNP Silicon Transistors
3. Microelectronics, Processes for Components of

I. LaRocque, Armond P. Yatsko, Robert S. Rogel, Alex Jackson, Raymond Rible, Vincent E.
II. Army Electronics Research and Development Laboratory, Fort Monmouth, N. J.
III. DA Task 3A99-21-003-02)

UNCLASSIFIED

UNCLASSIFIED

AD ______________ Div. ______________

Army Electronics Research and Development Laboratory, Fort Monmouth, N. J.
TECHNOLOGY FOR PNP PLANAR SILICON TRANSISTORS: SWITCHING & AMPLIFYING by Armond P. LaRocque, Robert S. Yatsko, Alex Rogel, Raymond Jackson, Vincent E. Rible, March 1963, 21 p. incl. illus. 5 refs. (USAELRDL Technical Report 2339) (DA Task 3A99-21-003-02)
Unclassified Report

Processes and techniques required for fabrication of experimental planar PNP silicon transistors have been developed and demonstrated as feasible. Processes involved include material preparation, antimony base diffusion, boron emitter diffusion, oxide masking, photoresist techniques, simultaneous gold metalizing of emitter and base regions, collector alloy contact and basing, and thermocompression bonding. Initial transistors have typical dc Beta values of 35 to 40 and F_T values as high as 350 MCS. Processes described have also been used in preliminary fabrication of solid-state micro-circuit passive components.

1. Transistors, PNP Silicon, Technology for
2. Technology, PNP Silicon Transistors
3. Microelectronics, Processes for Components of

I. LaRocque, Armond P. Yatsko, Robert S. Rogel, Alex Jackson, Raymond Rible, Vincent E.
II. Army Electronics Research and Development Laboratory, Fort Monmouth, N. J.
III. DA Task 3A99-21-003-02)

UNCLASSIFIED

AD ______________ Div. ______________

UNCLASSIFIED

Army Electronics Research and Development Laboratory, Fort Monmouth, N. J.
TECHNOLOGY FOR PNP PLANAR SILICON TRANSISTORS: SWITCHING & AMPLIFYING by Armond P. LaRocque, Robert S. Yatsko, Alex Rogel, Raymond Jackson, Vincent E. Rible, March 1963, 21 p. incl. illus. 5 refs. (USAELRDL Technical Report 2339) (DA Task 3A99-21-003-02)
Unclassified Report

Processes and techniques required for fabrication of experimental planar PNP silicon transistors have been developed and demonstrated as feasible. Processes involved include material preparation, antimony base diffusion, boron emitter diffusion, oxide masking, photoresist techniques, simultaneous gold metalizing of emitter and base regions, collector alloy contact and basing, and thermocompression bonding. Initial transistors have typical dc Beta values of 35 to 40 and F_T values as high as 350 MCS. Processes described have also been used in preliminary fabrication of solid-state micro-circuit passive components.

1. Transistors, PNP Silicon, Technology for
2. Technology, PNP Silicon Transistors
3. Microelectronics, Processes for Components of

I. LaRocque, Armond P. Yatsko, Robert S. Rogel, Alex Jackson, Raymond Rible, Vincent E.
II. Army Electronics Research and Development Laboratory, Fort Monmouth, N. J.
III. DA Task 3A99-21-003-02)

UNCLASSIFIED

UNCLASSIFIED

AD ______________ Div. ______________

Army Electronics Research and Development Laboratory, Fort Monmouth, N. J.
TECHNOLOGY FOR PNP PLANAR SILICON TRANSISTORS: SWITCHING & AMPLIFYING by Armond P. LaRocque, Robert S. Yatsko, Alex Rogel, Raymond Jackson, Vincent E. Rible, March 1963, 21 p. incl. illus. 5 refs. (USAELRDL Technical Report 2339) (DA Task 3A99-21-003-02)
Unclassified Report

Processes and techniques required for fabrication of experimental planar PNP silicon transistors have been developed and demonstrated as feasible. Processes involved include material preparation, antimony base diffusion, boron emitter diffusion, oxide masking, photoresist techniques, simultaneous gold metalizing of emitter and base regions, collector alloy contact and basing, and thermocompression bonding. Initial transistors have typical dc Beta values of 35 to 40 and F_T values as high as 350 MCS. Processes described have also been used in preliminary fabrication of solid-state micro-circuit passive components.

1. Transistors, PNP Silicon, Technology for
2. Technology, PNP Silicon Transistors
3. Microelectronics, Processes for Components of

I. LaRocque, Armond P. Yatsko, Robert S. Rogel, Alex Jackson, Raymond Rible, Vincent E.
II. Army Electronics Research and Development Laboratory, Fort Monmouth, N. J.
III. DA Task 3A99-21-003-02)

UNCLASSIFIED